

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): HASEGAWA, et al.

Application No.: TBD

Filed: October 1, 2003

For: METHOD OF MANUFACTURING SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE, OPTICAL MASK THEREFOR, ITS MANUFACTURING METHOD, AND MASK BLANKS

Expected Group: 1756

Expected Examiner: Saleha R. Mohamedulla

CLAIM FOR PRIORITY

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

October 1, 2003

Sir:

Pursuant to the requirements of 35 USC §119 and 37 CFR §1.55, Applicants claim priority based upon Japanese Patent Application No. 11-185221, filed in Japan on June 30, 1999.

As acknowledged in the Office Action Summary of the Office Action mailed January 21, 2003, in prior Application No. 09/646,036, filed September 13, 2000, the necessary certified copy of the priority document has been received at the U.S. Patent and Trademark Office.

Respectfully submitted,

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WIS/sjg